**Projeto 1 - Lab. de Sistemas Digitais**

***Alunos:*** *Henrique Vieira Lima - 15459372*

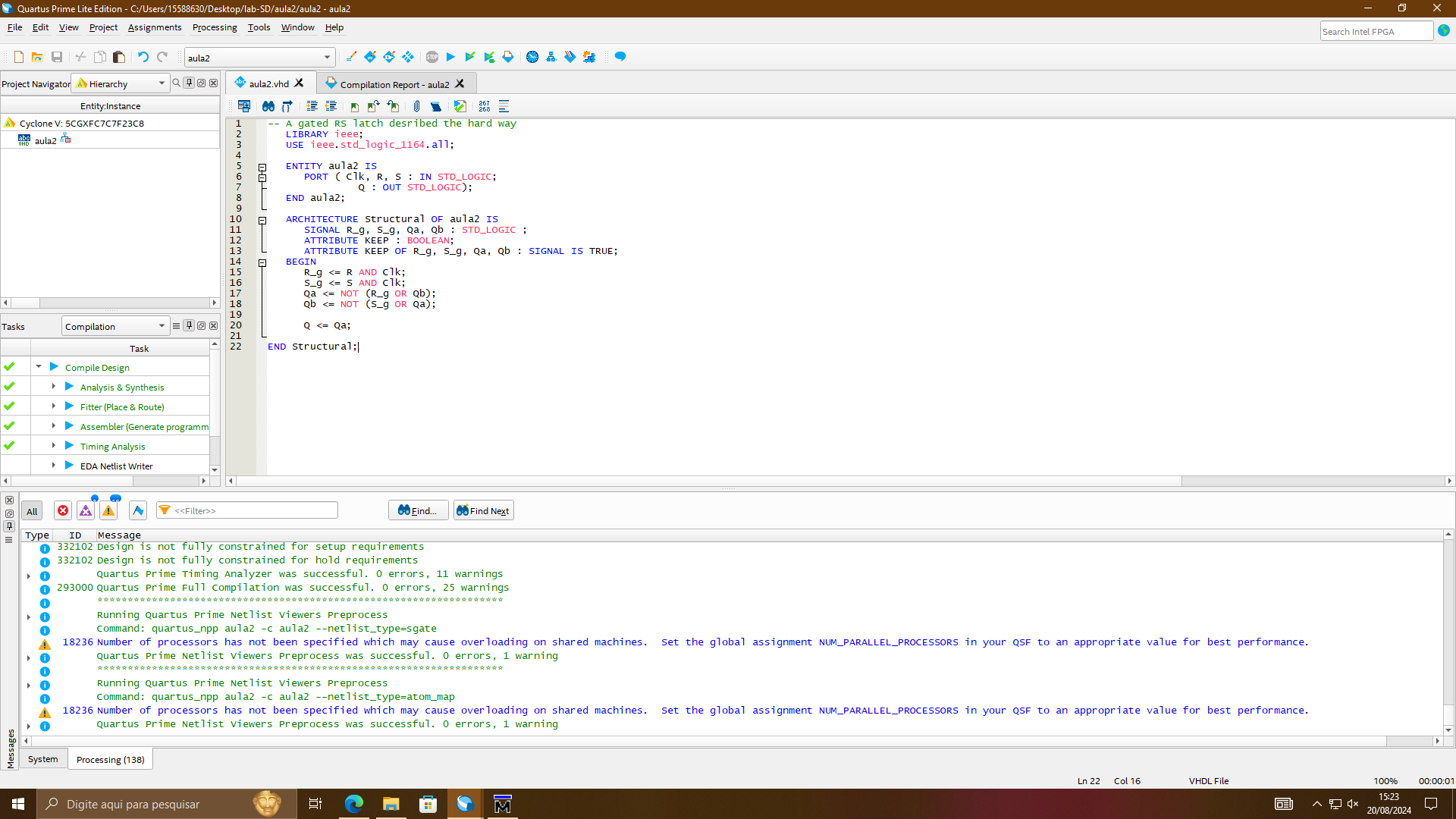
*Beatriz Alves dos Santos - 15588630*

***Data:*** *20/08/2024*

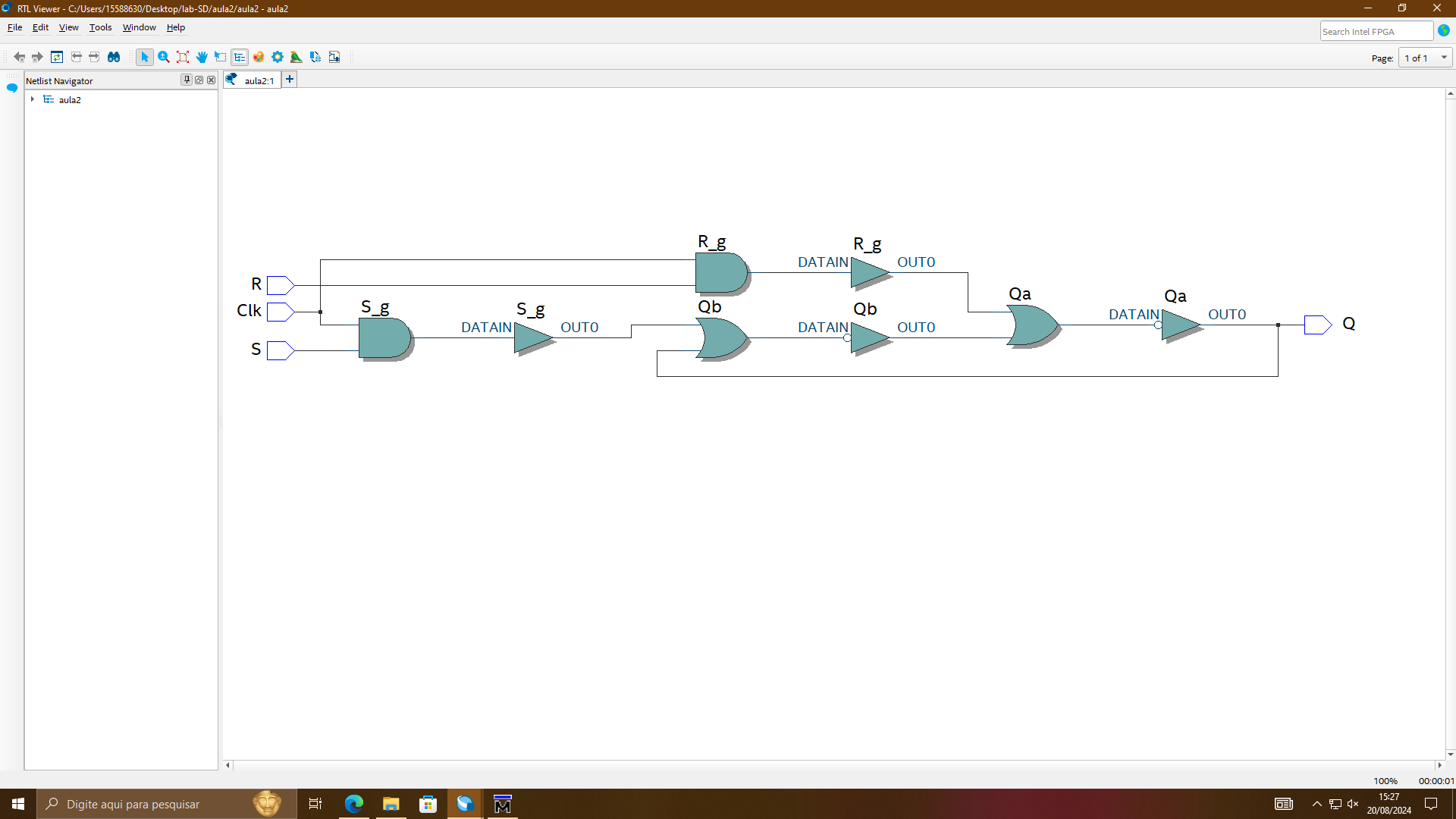
***Placa:***(Placa Grande) DE2-115 - Cyclone IV E: EP4CE115F29C7

**Parte 1**

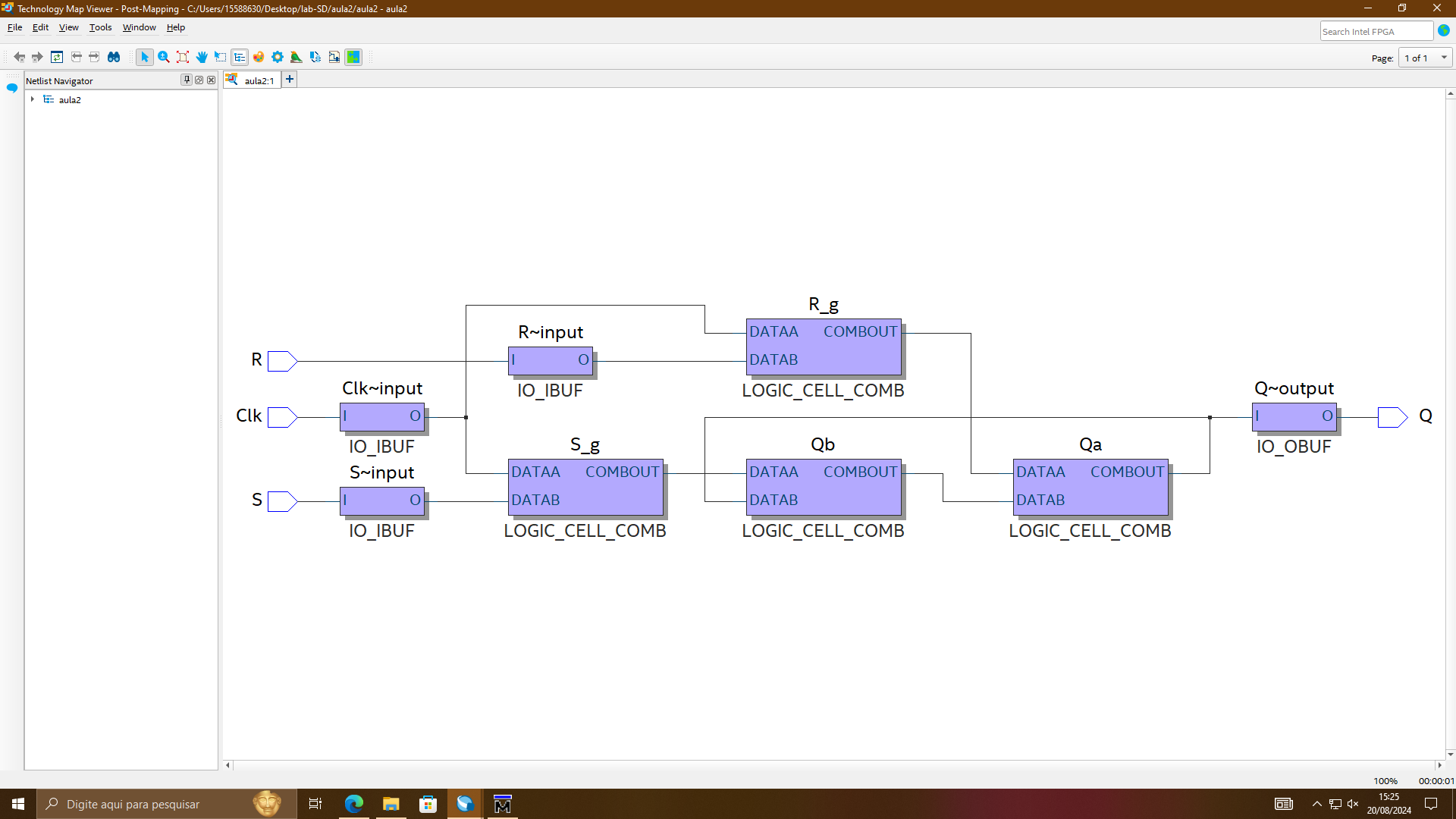
Código VHDL:



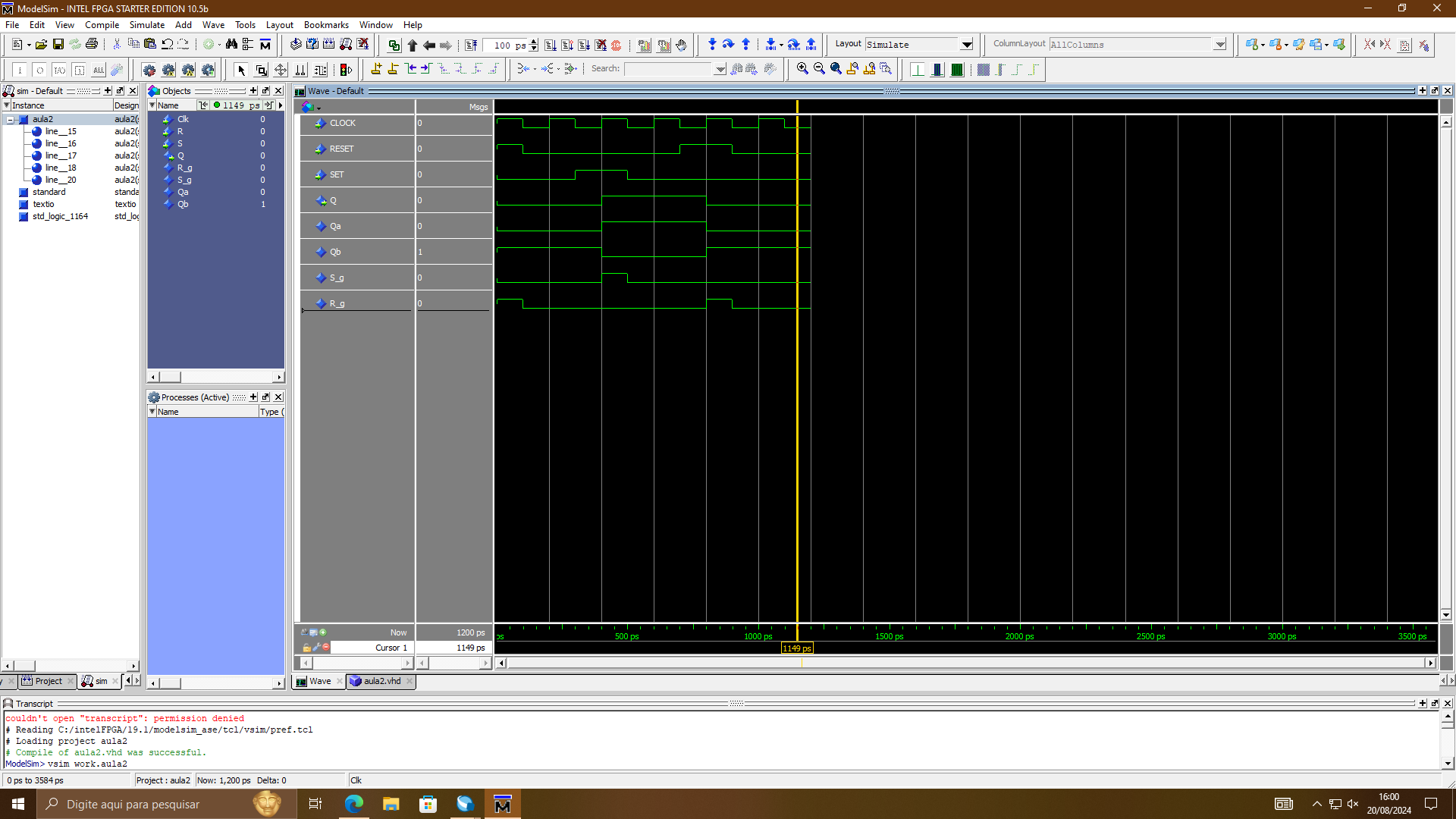
Circuito portas lógicas (RTL Viewer):



Map Technology Viewer:

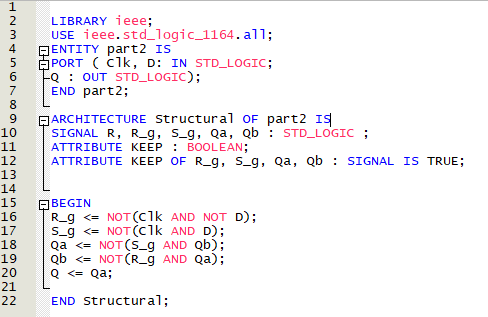


Simulação de ondas (ModelSim):

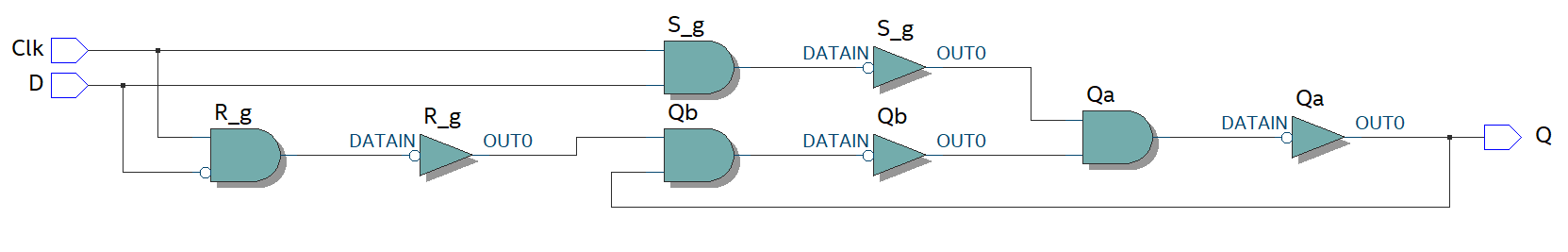


**Parte 2**

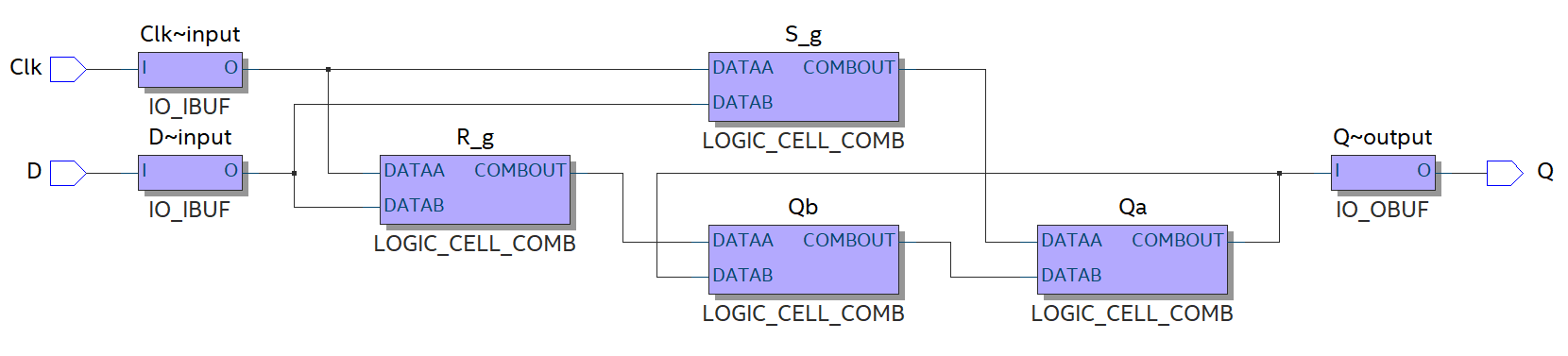
Código VHDL:

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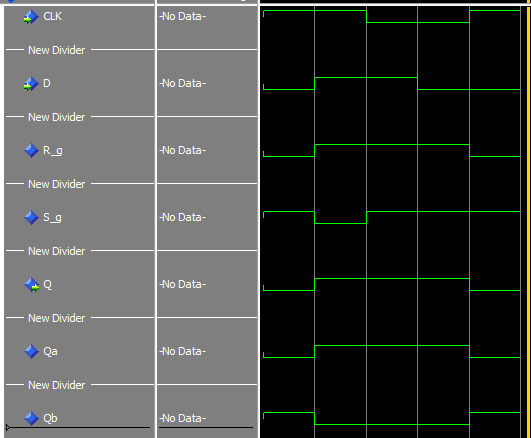
Circuito portas lógicas (RTL Viewer):



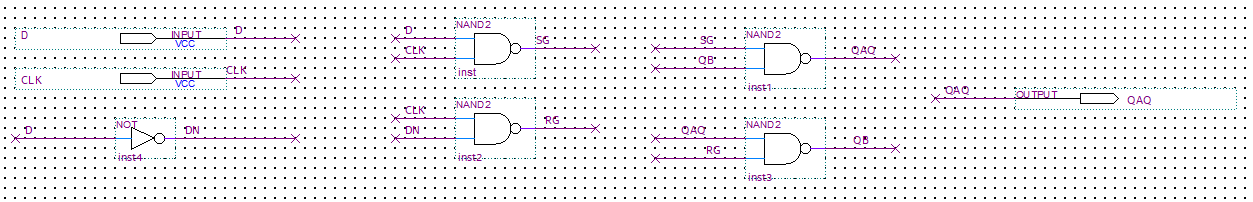
Map Technology Viewer:



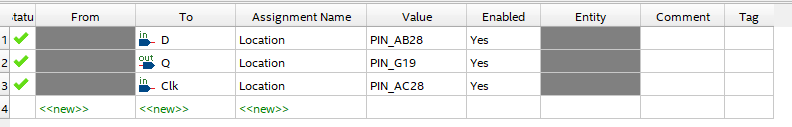
Simulação de ondas (ModelSim):

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Circuito Quartus:

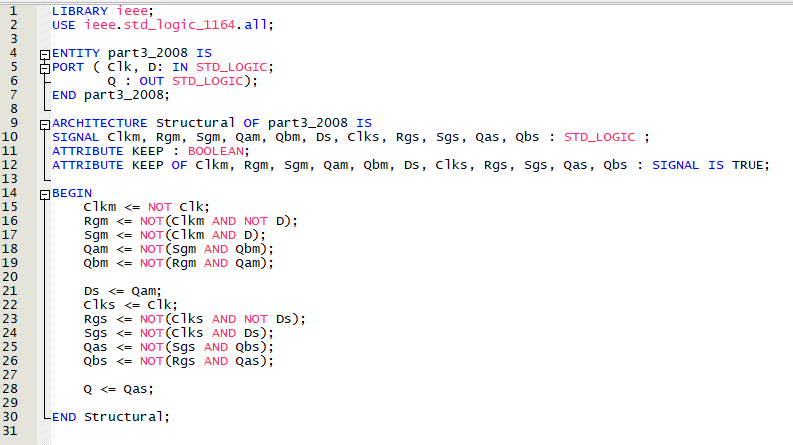
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Assignments:

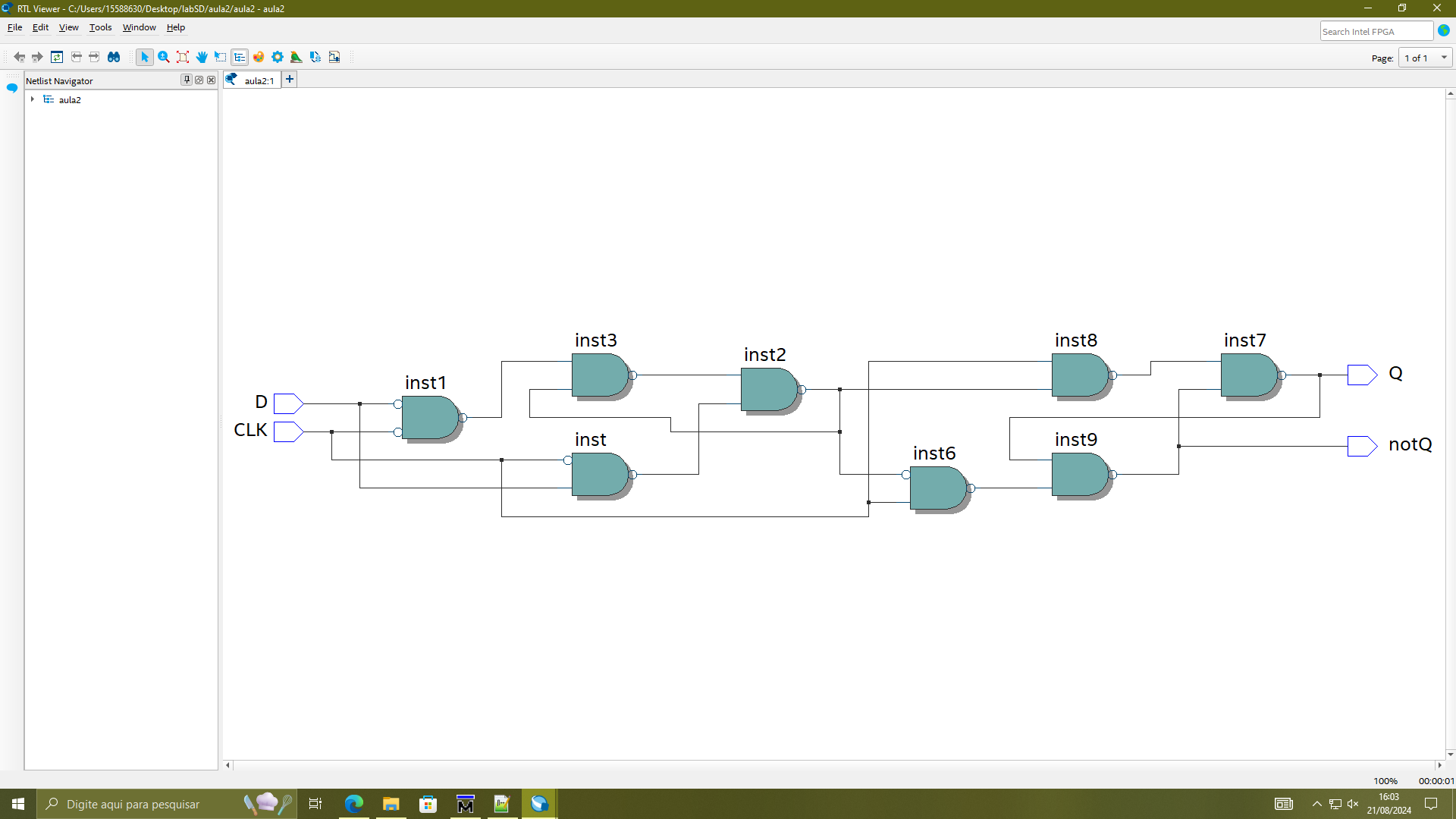


**Parte 3**

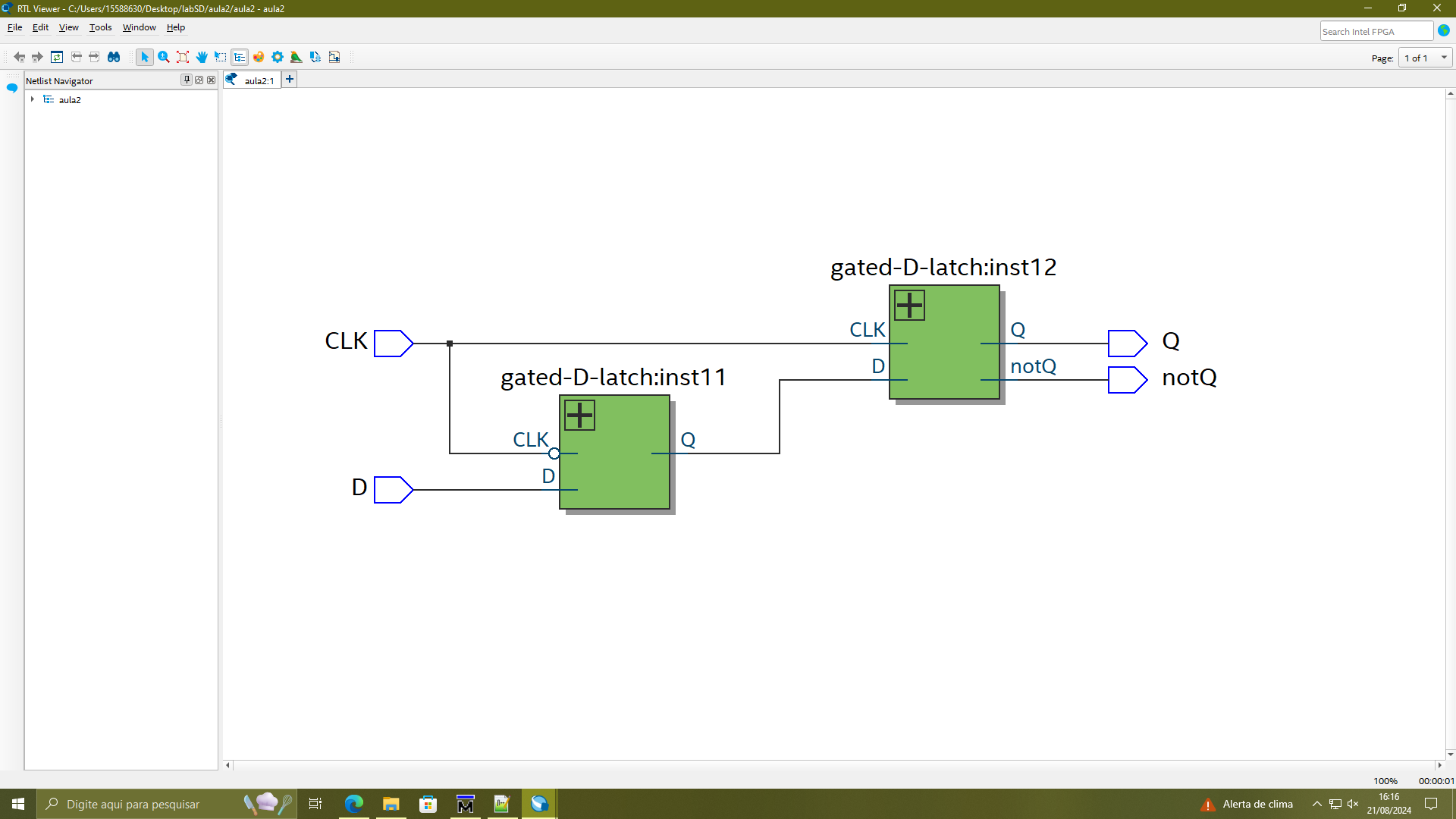
Código VHDL:

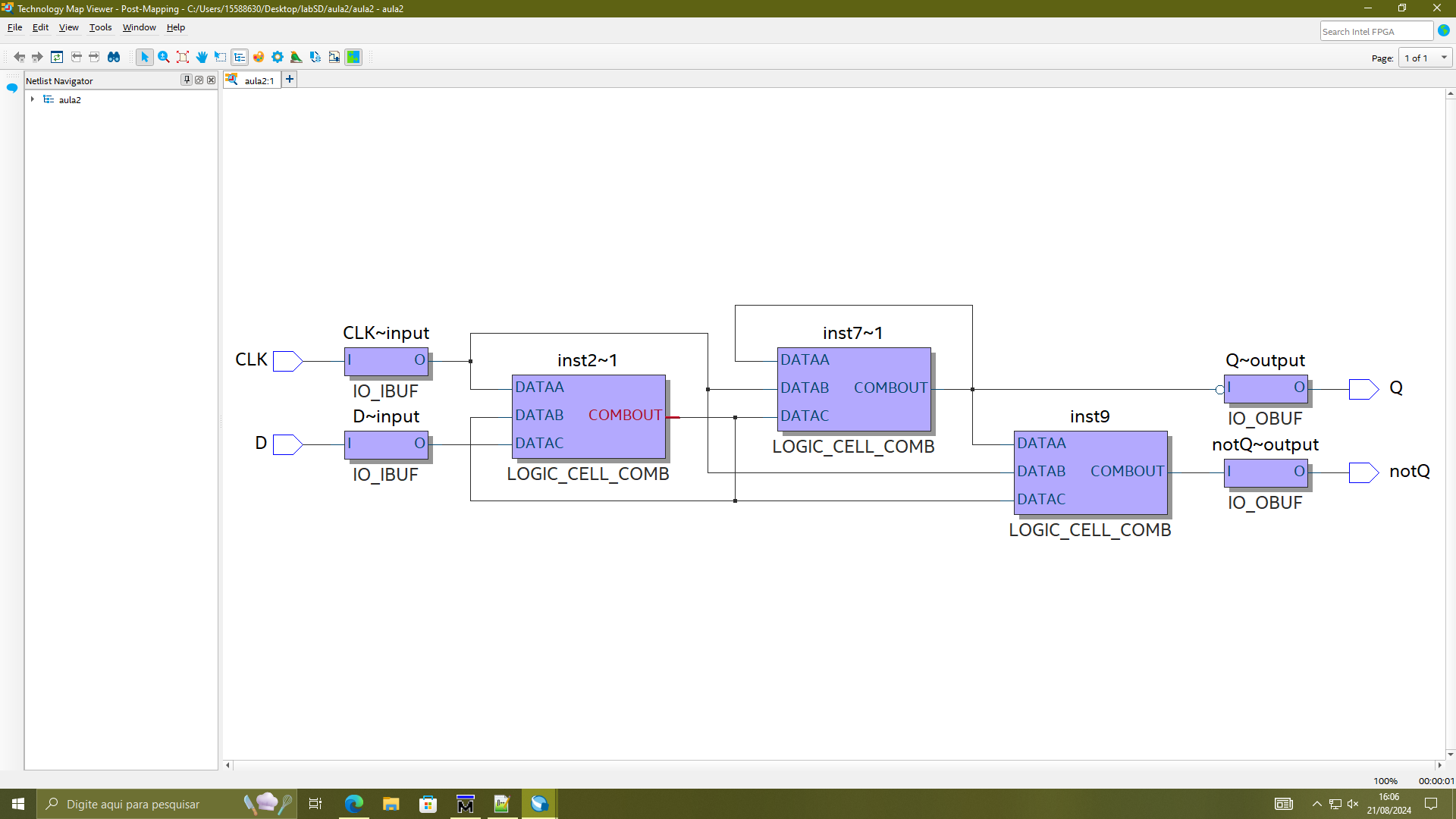
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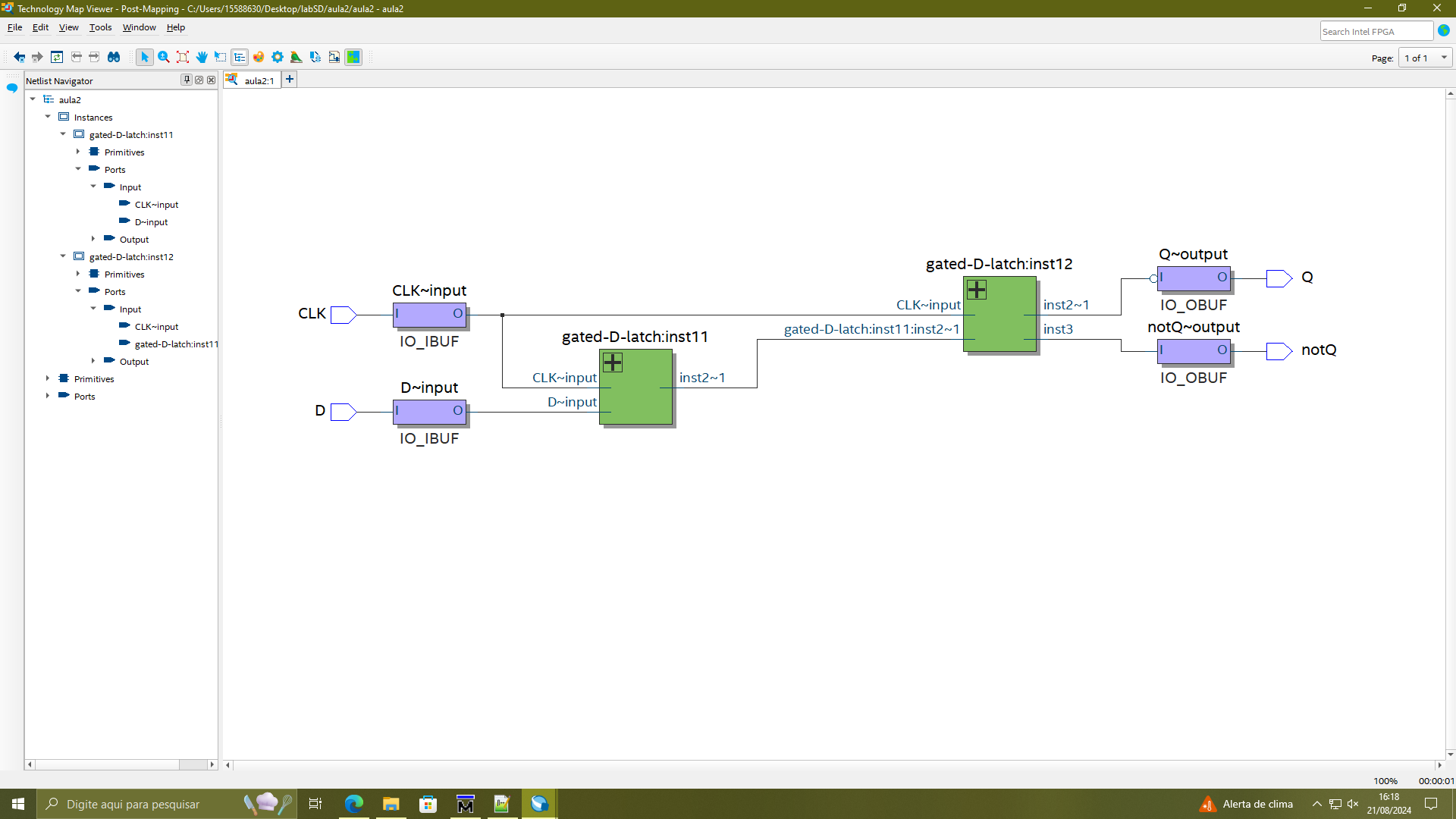
Circuito portas lógicas (RTL Viewer):



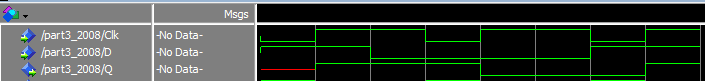
Com blocos:



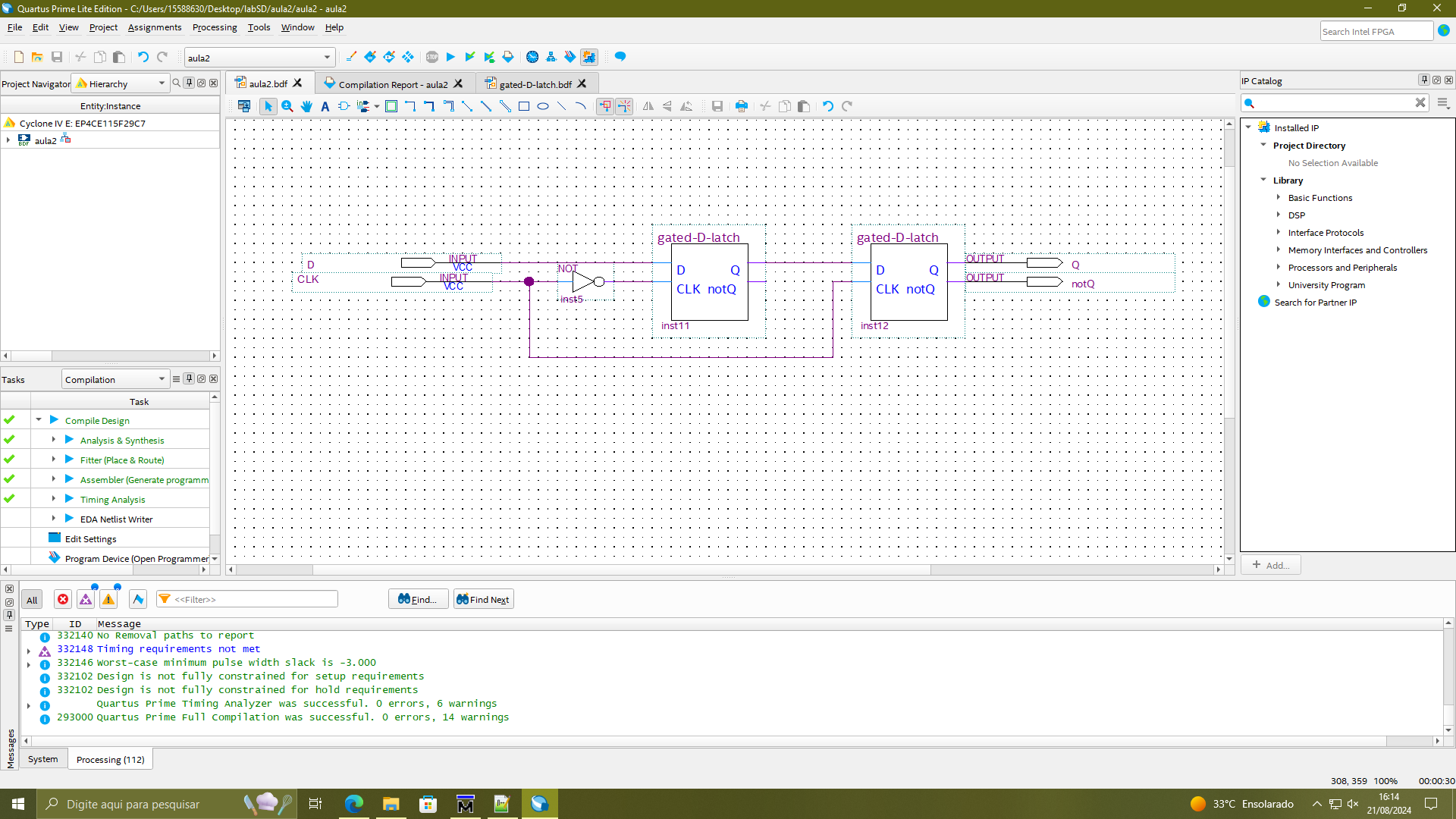
Map Technology Viewer:

Com blocos:

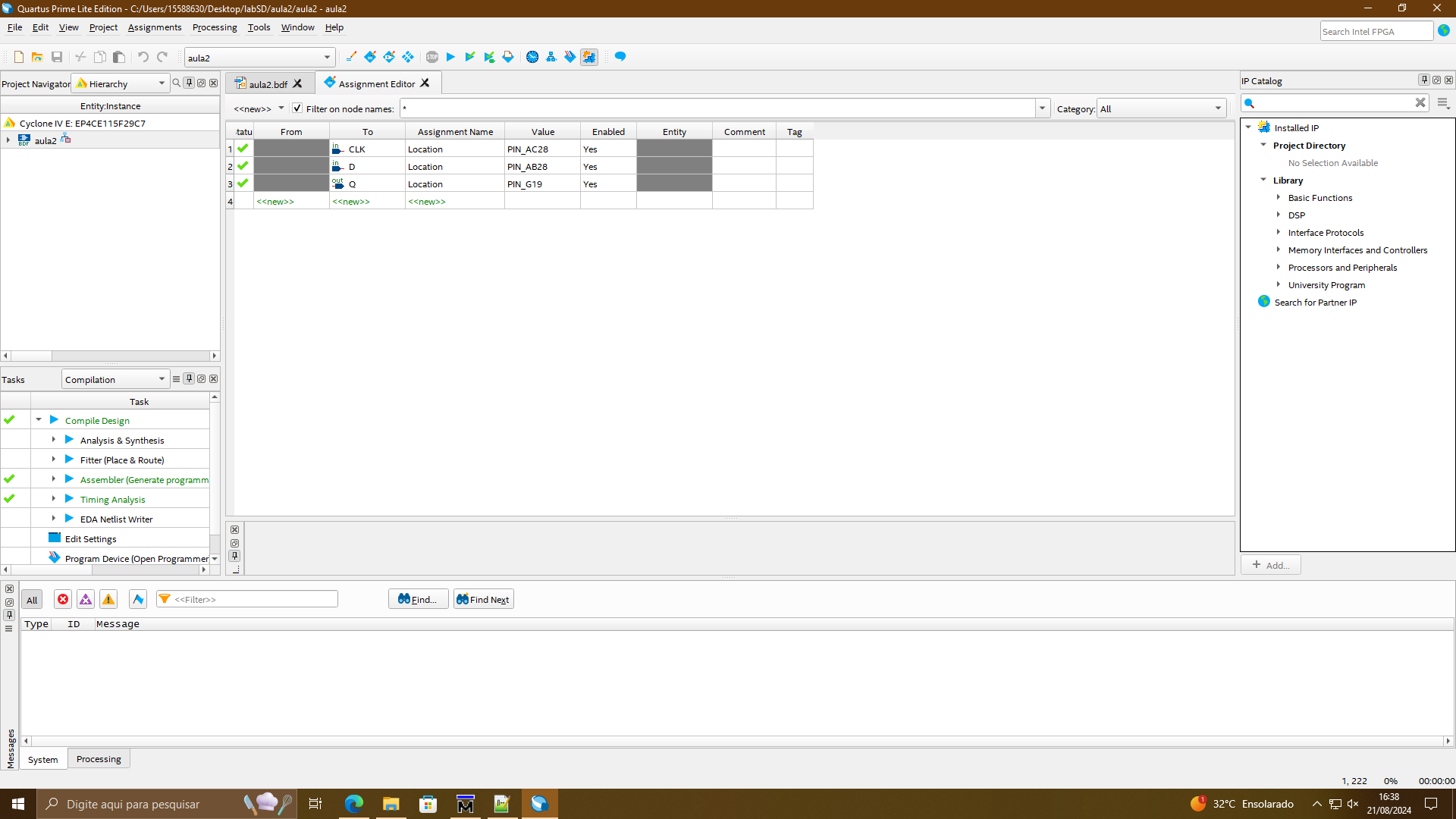
Simulação de ondas (ModelSim):

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Circuito Quartus:

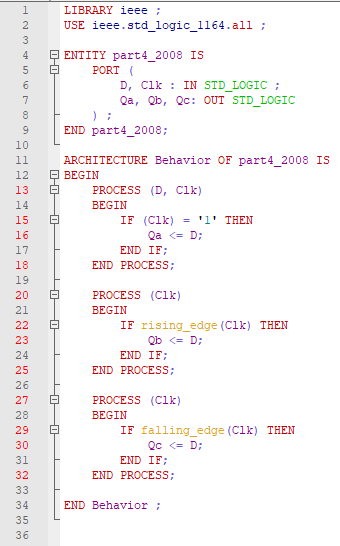
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Assignments:

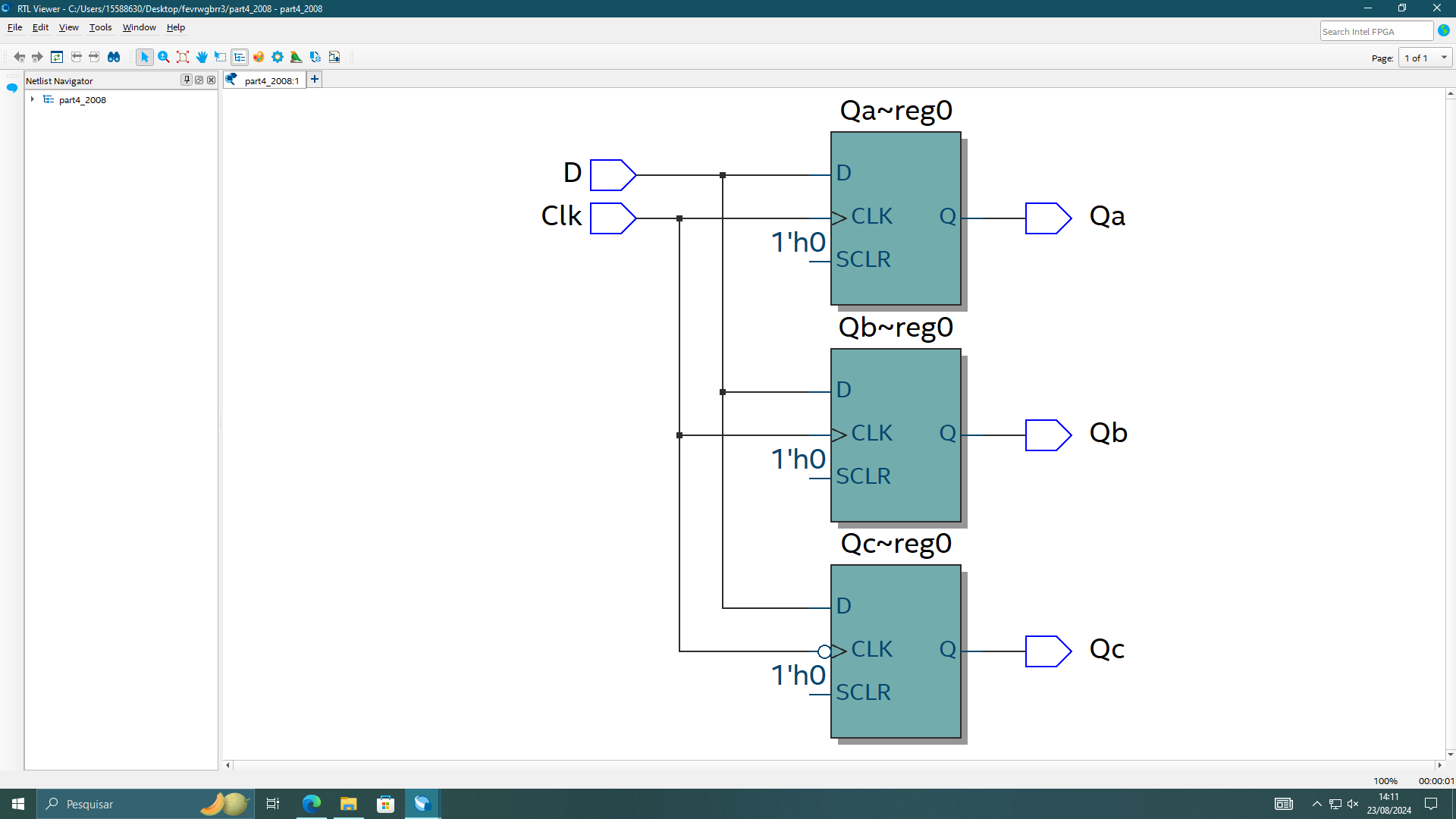


**Parte 4**

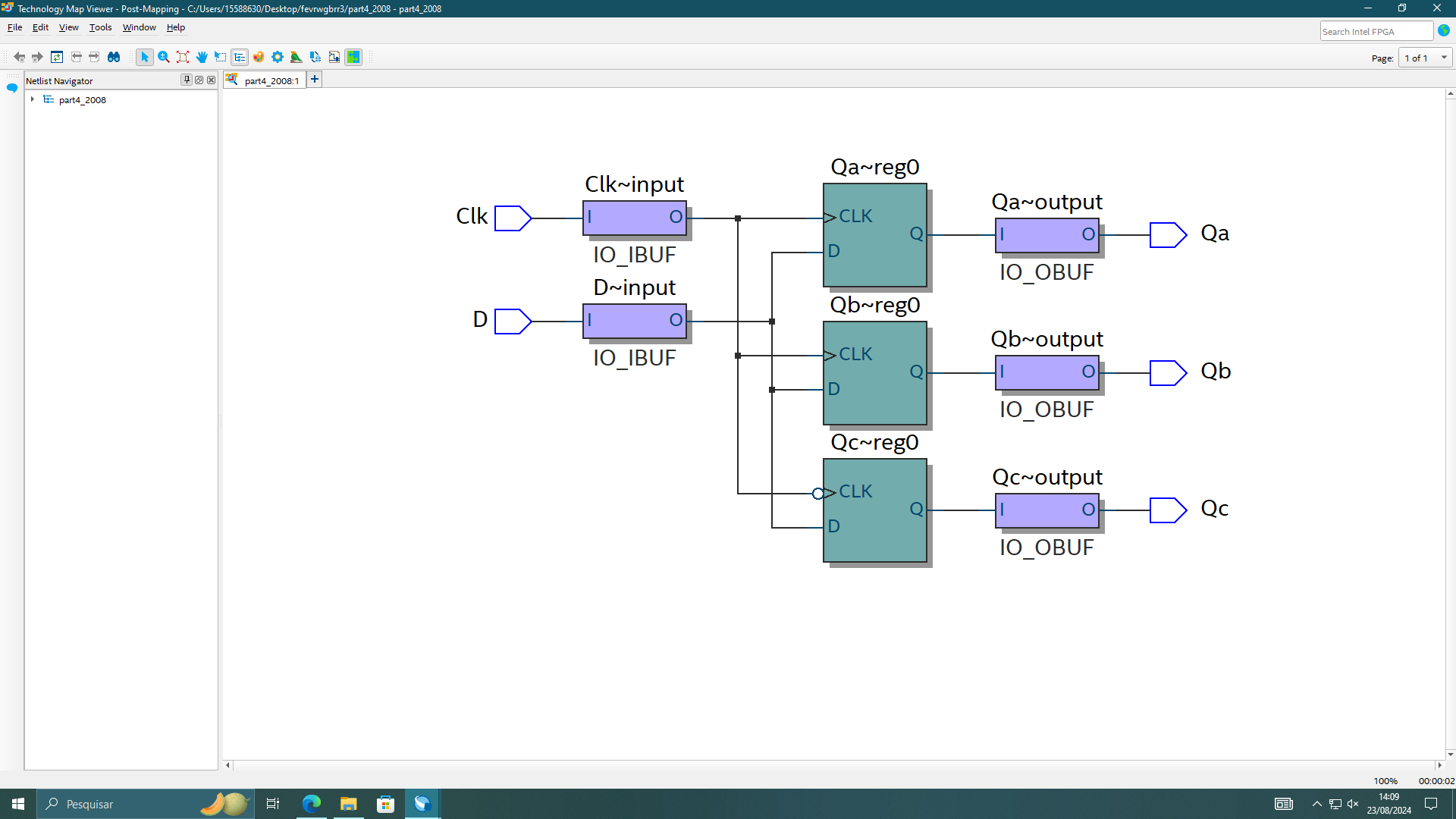
Código VHDL:

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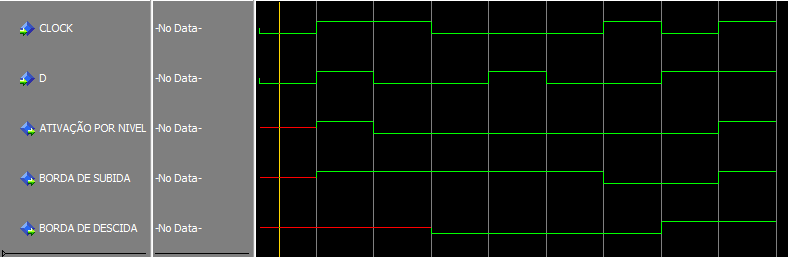
Circuito portas lógicas (RTL Viewer):



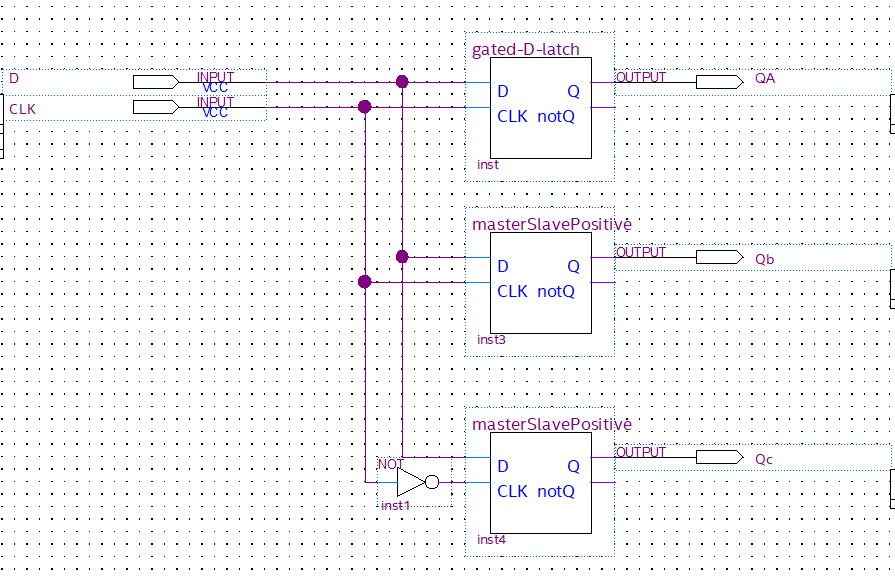
Map Technology Viewer:



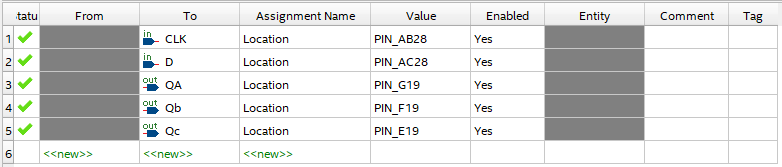
Simulação de ondas (ModelSim):

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Circuito Quartus:

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Assignments:

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